CREATING PHOTOLITHOGRAPHIC MASKS

CROSS-REFERENCE TO RELATED APPLICATIONThis application is a continuation of Application No. 09/703,294, filed October 31, 2000, which is incorporated herein by reference.

FIELD OF THE INVENTION

The present invention relates to photolithographic processing.

BACKGROUND OF THE INVENTION

In order to create faster and more powerful integrated circuits, circuit designers are increasing the number and decreasing the size of circuit elements that are placed on an integrated circuit. With conventional photolithography, the minimum size of an object that can be created on a silicon wafer depends directly on the wavelength of light used to expose the wafer and inversely on the numerical aperture of the lens through which the light that exposes the wafer is passed. Because the costs associated with decreasing the illumination wavelength or increasing the numerical aperture can be prohibitive, chip manufacturers are continually looking for techniques that can create smaller objects on a wafer using existing photolithographic equipment.

One of the most powerful techniques for increasing the density of an integrated circuit with existing photolithographic equipment is with the use of phase shifters. As discovered by Marc Levenson of IBM and others, the phase of the light that strikes a wafer can be manipulated to destructively interfere at desired locations on the wafer in order to enhance image contrast and reduce diffraction effects that occur when the light passes through a pattern of opaque areas on a semiconductor

mask. In addition, by selectively placing phase shifters on the mask, subwavelength features can be created on the wafer to form circuit elements.

While the use of phase shifting structures on a photolithographic mask allows increased contrast and the creation of subwavelength features using existing photolithographic equipment, the phase shifters are relatively expensive to create and may introduce errors into the mask. Therefore, there is a need for a method and apparatus for optimizing the creation of phase shifters on a mask that minimizes the possibility of errors and facilitates the production of the mask.

SUMMARY OF THE INVENTION

A method and apparatus for optimizing data used in the creation of a photolithographic mask. The apparatus includes a computer system for reading data that describes a desired physical layer of an integrated circuit. The computer creates multiple data layers and groups data structures that define different areas on the mask into one of the multiple data layers. After the data structures are defined and grouped into one of the data layers, the data structures grouped in one or more of the data layers are analyzed according to one or more design rules. One or more properties of the data structures are then assigned in accordance with the analysis performed.

In a currently preferred embodiment of the invention, the invention is used to optimize data that defines phase shifters on a photolithographic mask. The computer system creates data structures that define polygons that correspond to circuit elements and polygons that correspond to phase shifters on the mask. Polygons are then placed in one of the corresponding data layers. All the polygons associated with circuit features are grouped in one data layer and the polygons associated with distinct phase shift areas are grouped in separate data layers. The phase shifting polygons in the data layers are analyzed and a phase shift amount is assigned to each of the polygons after the polygons have been created, and based on the design rule analysis. In one embodiment of the invention, the design rules operate to minimize an etched area of the mask.

The present invention is not limited to the optimization of data used to create masks for integrated circuits. The present invention can also be used to optimize data used to create micro electro-mechanical structures (MEMS), thin film heads for disk drives or other devices created with photolithographic processes.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same become better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIGURES 1A-1H illustrate cross sections of various types of known phase shifting elements that may be incorporated into a photolithographic mask;

FIGURES 2A and 2B illustrate a portion of a desired circuit and how phase shift values are conventionally assigned to adjacent phase shifting areas on a mask;

FIGURE 3 is a flow chart of the conventional steps performed to assign phase shift values to areas of a phase shifter;

FIGURES 4A-4B illustrate a flow chart of the steps performed by one embodiment of the present invention to optimize the assignment of phase shift values to areas of phase shifters;

FIGURE 5 illustrates a computer system for performing the method outlined in FIGURE 4;

FIGURES 6A-6G illustrate a portion of a desired circuit and how the present invention optimizes the assignment of phase shift values; and

FIGURE 7 illustrates the use of the present invention with attenuated phase shifters.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

As indicated above, the present invention is a method and apparatus for optimizing data for the creation of circuit elements on a photolithographic mask and, in particular to the optimization of data for the creation of phase shifters on a photolithographic mask.

FIGURES 1A-1H illustrate various types of structures commonly used on photolithographic masks. As shown in FIGURE 1A, a mask 10 typically comprises a transparent substrate, typically quartz or glass, having a number of opaque areas 12, typically fabricated from chrome, disposed on one surface thereof. This is typically called a conventional, chrome-on-glass (COG) mask. The mask 10 is placed into a wafer processing machine whereby light is passed through the mask 10 and an image of the mask is formed on the surface of a silicon wafer (not shown) that is covered with a photosensitive material. The light exposes portions of the photosensitive material and the exposed/unexposed areas of the photoresist material are then

processed in order to create a pattern on the wafer corresponding to the pattern of opaque areas 12 on the corresponding mask 10.

In order to improve the contrast between adjacent features on the wafer or to create features that are smaller than the wavelength of the light used to expose the wafer, the mask 10 may include one or more phase shifters, as shown in figure 1B. Light passing directly through a transparent area of the mask 10 as indicated by the beam 14 forms a reference against which the phase of phase shifted illumination light is compared. Clear areas of the mask are typically referred to as zero degree (0°) areas. The phase of the light passing through the mask 10 may be adjusted by adding a layer of transparent material 16 to the surface of the mask 10. The thickness of the material 16 added can be varied in order to control the phase of the light passing through that area of the mask 10 with respect to the phase of the light passing through a 0° area of the mask 10. For example, light passing through an additional layer of material 16, as indicated by the beam 18, is 180° out of phase with the light beam 14. When light beams that are 180° out of phase intersect on the silicon wafer, the lightwaves destructively interfere, thereby enhancing the contrast between exposed portions on the wafers that are created by adjacent opaque areas 12 on the mask 10.

The phase of the light passing through the mask also can be adjusted by etching an area into the mask in order to reduce its thickness. FIGURE 1C shows a mask 10 having an area 20 that has been etched to shift by 180° the phase of the light passing through the area as indicated by the light beam 22.

As long as the relative phase shift between adjacent phase shifting areas is 180°, the contrast enhancement is still achieved. FIGURE 1D shows a mask 10 having an area 24 that has been etched to shift the phase of the illumination light by 90° with respect to light that passes through a 0° area of the mask. The mask 10 also includes an area 26 that is etched to shift the phase of the illumination light by 270°. Light passing through a 0° area, indicated by the light beam 14, and a 90° area, as indicated by the light beam 28, will not destructively interfere to create a sub-wavelength feature on the wafer. Similarly, light passing through the 270° phase shift area, as indicated by the light beam 30, will not destructively interfere with light passing through a 0° portion of the mask 10 to create sub-wavelength features. Only light passing through adjacent 90° and 270° phase shift areas will create sub-wavelength features. Using 90° and 270° phase shifters allows greater flexibility in the layout of phase shifting masks. However, having phase shifters etched to

different depths on the mask generally makes the mask more expensive to manufacture.

The use of phase shifters is not limited to enhancing the contrast between adjacent apertures separated by opaque areas on a mask. A phase shifting area can be placed inside a clear area on the mask in order to create sub-wavelength features on the wafer. FIGURE 1E illustrates a mask 10 having a 0° area 34 that is adjacent a 180° phase shift area 36. Light passing through these areas, as indicated by the beams 38 and 40, destructively interfere at the wafer thereby producing an unexposed pattern that can form a desired element on the wafer.

As is well known to those of ordinary skill in the art, at each location on the mask where a 180° phase shift area borders a 0° phase shift area, destructive interference will create a sub-wavelength feature on the wafer. Because each phase shifting region must have a closed boundary, additional features may appear in undesirable locations. These undesired features can be removed with a trim mask 11 having opaque areas 39, 41, as shown in FIGURE 1F that shield desired portions of the sub-wavelength features and expose undesired portions of the sub-wavelength features.

FIGURE 1G illustrates the use of multiple adjacent phase shifting areas on a mask 10. The mask 10 includes a 0° phase shifting area 42 that is adjacent to a 180° phase shifting area 44 that, in turn, is adjacent a sequence of 90° phase shifting areas 46. Light passing through the 0° and 180° degree areas, as indicated by beams 48 and 50, will destructively interfere on the wafer to create a sub-wavelength unexposed area. Light passing through the 180° phase shift area indicated by the beam 50 and the 90° phase shift area as indicated by the beam 52 or at the boundary of the 90° and 0° regions will not interfere to create a sub-wavelength feature. Thus, placing a 90° phase shift area between a 0° and a 180° phase shift area on the mask 10 can reduce or eliminate the unwanted sub-wavelength features that would otherwise be created at the boundaries of a 180° and 0° phase shift area without a trim mask. However, these masks are more complex and therefore more expensive.

An alternate approach of creating a phase shifter is to alter the material used to make the opaque patterns on the mask 10. Such patterns are generally created with opaque chromium. By making the chromium thin enough, or using specially developed partially transmitting materials such as Molybdenum silicide, the material becomes semi-transparent and alters the phase of the light passing through it by 180°, but decreases its amplitude. FIGURE 1H shows a mask 10 having a 0° phase shift

area 56 and a semi-transparent pattern 58. Light passing through the semi-transparent pattern 58 is shifted 180° with respect to light passing through the 0° area 56 of the mask in order to enhance the contrast between adjacent features. Uniform phase shifting can be achieved by creating a uniform layer of the material.

As will be appreciated, the semi-transparent pattern 58 increases the overall amount of light that reaches the wafer. Therefore, portions of the semi-transparent pattern may be covered with an opaque chrome layer to produce a "tri-tone" mask as will be described in further detail below.

While the use of phase shifters permits integrated circuits with an increased density to be created with existing photolithographic equipment, their use generally increases the cost of producing the mask and may introduce errors into the mask. FIGURES 2A-2B and 3 illustrate the conventional method by which phase shifters are added to a photolithographic mask. FIGURE 2A shows a portion of a desired circuit to be created on a silicon wafer. The circuit includes a number of polysilicon elements 80a-80e that are large enough to be created by a conventional COG photolithographic mask. In addition, the circuit includes two gates 82a and 82b that are sub-wavelength features.

To prepare the data for a mask that will create the desired layout on a silicon wafer, the process steps shown in FIGURE 3 are usually performed. It should be noted that the term "mask" in photolithographic processing technically refers to an object that is placed in direct contact with a wafer during processing, as opposed to a reticle which is positioned at some distance away from the wafer during processing. However, for purposes of the present specification, the term "mask" is intended to have its more colloquial definition and refer to both contact masks and reticles. Beginning with a step 100, a computer file containing a description of the circuit layout is received and provided to a layout manipulation program. A layout manipulation and verification program takes the description of the circuit elements and defines a number of polygons that in turn correspond to areas on one or more photolithographic masks at a step 102. For example, to create the circuit element 80a, the layout manipulation program defines a polygon p80a (FIGURE 2B) that describes the dimensions of a portion of a mask that will create the element 80a when the mask is illuminated. In addition, the layout manipulation program detects that the gates 82a and 82b are too small to be created using a convention mask and therefore generates polygons that ensure that the mask includes phase shifting regions 84, 86 and 88 that will create these sub-wavelength features by destructive

interference. The description of the polygons that define areas the mask is generally referred to as a GDS II data layer for the format of a language commonly used to describe the polygons, although other data formats can also be used.

At a step 104, the layout manipulation program makes an initial phase selection for one of the phase shift areas. For example, if the circuit designer selects a design using 0° and 180° phase shift areas, the layout manipulation program will select either 0° or 180° as the phase shift for the first area. Processing then continues at a step 106 where the layout manipulation program continues through the data layer assigning each phase shift area a phase shift amount that is the opposite of its neighboring phase shift area. In the example shown in FIGURE 2, the phase shift area 86 is assigned 180° of phase shift and the area 88 is assigned 0° of phase shift.

The problem with the approach shown in FIGURES 2B and 3 is that the arbitrary phase assignments that can occur when simple rules are executed for the assignment of phase shift values at the same time the polygons are generated can result in sub-optimal masks. For example, masks with large etched areas may contribute to errors on the mask. As shown in FIGURE 2B, the area 86 that is etched to produce 180° of phase shift completely contains the polygon p80e. Having an etched area that completely surrounds a chrome feature on the mask can cause etching of the chrome itself, changing the dimensions and increasing the number of defects on the mask. Repair of these defects may be difficult and time consuming, increasing the cost of the mask.

To improve the creation of phase shift areas on a mask, one embodiment of the invention performs the steps shown in FIGURES 4A-4B. Beginning with a step 120, the data layer for a selected physical chip layer is obtained. For example, the physical chip layer may be the polysilicon device layer that specifies a particular pattern of transistors to be created on the wafer. At a step 122, a layout manipulation program, such as is part of Calibre™ produced by Mentor Graphics Corporation of Wilsonville, Oregon, the assignee of the present invention, is executed by a computer system to determine the appropriate phase shifting method - either by prompting a user to make a selection or based on one or more design rules. At a step 124, the computer creates a number of data layers depending on the type of phase shifters to be used. For example, if a 0° and 180° phase shifting scheme with double exposure is used, the computer system creates four data layers. One data layer is created for the circuit elements that can be created with conventional patterns formed on a mask, one data layer is created for each phase shifting portion of the phase shifters, as will

be explained below, and one data layer is created for a trim mask. If a 90°/270° phase shifting scheme is used, the computer system creates three data layers since no trim mask is needed. It should be noted that the data layers do not correspond to distinct layers of the circuit to be fabricated as distinct masks, but correspond to separate data structures such as arrays, files or other storage mechanisms in which the polygons grouped therein can be analyzed. At the time of creation, these data layers are generally empty, and do not yet contain any polygons.

At a step 126, the layout manipulation program creates those polygons that define different phase shifting areas of the phase shifters and places them into one of the different data layers created.

Selecting an actual phase shift amount for each of the polygons in the different data layers does not yet occur. Preferably, after the polygons are created, the assignments made. At a step 128, the layout manipulation program makes a phase shift selection for all the phase shift polygons in the same data layer in accordance with a desired design criteria. For example, it may be advantageous to minimize the area of the 180° phase shift areas on the mask. Therefore, the layout manipulation program sums the area of each phase shifting polygon included in each data layers. The polygons in the data layer having the minimum combined area can be defined as the 180° phase shift regions. Alternatively, the selection of which polygons define the 180° phase shift areas may be made based on other design criteria, such as proximity to circuit elements in other layers, or the predictive results of a simulation algorithm.

At a step 130, the layout manipulation program may run a simulation of the circuit based on the phase assignments made at step 128. At a step 132, it is determined if the simulation is acceptable. If not, processing can proceed to a step 134 and selected phase shifting polygons can be reassigned to another data layer or the phase shift assignment for the entire data layer can be changed. After step 134, processing returns to step 130 and the simulation is performed again. Once the simulation is acceptable, processing proceeds to a step 136, whereby the polygon definitions for each of the data layers is provided as input to a mask writer to create the mask for the physical chip layer.

FIGURE 5 illustrates the basic components of a hardware system that implements the present invention. A database 150 stores GDS II layer data for each physical layer of an integrated circuit to be created. The data is read by a computer system 152 that executes a program that implements the functions outlined in

FIGURES 4A-4B and described above. Once the data layers have been created, the polygon definitions have been divided among the data layers and the phase assignments for the phase shifting areas selected and the design verified, the polygon definitions in each data layer are supplied as input to a mask data processor 154 that controls the production of the actual photolithographic mask.

FIGURES 6A-6G illustrate how one embodiment of the present invention operates with an actual circuit design. FIGURE 6A illustrates a portion of a desired integrated circuit design including a number of circuit elements 200a-200e that are large enough to be created with conventional mask patterns. In addition, the desired circuit design includes a gate 202a that connects element 200a with element 200c and a gate 202b, which connects circuit element 200b with circuit element 200d. In the example shown in FIGURE 6A, gates 202a, 202b are too small to be created with a conventional mask. Therefore, the layout manipulation program knows that these elements must be created with the use of phase shifters.

FIGURE 6B illustrates polygons created by the layout manipulation program in order to produce the mask or masks that will in turn be used to create the circuit elements shown in FIGURE 6A. The layout manipulation program defines a series of polygons p200a-p200e that correspond to the circuit elements 200a-200e, respectively. Each of these polygons, for example polygon p200a, defines an area on the mask that will create the corresponding element 200a on the wafer without the use of the phase shifter. If the mask is a bright field mask, the polygon p200a will be defined as an opaque area on the mask surrounded by clear or 0° phase shift areas. If the mask is a dark field mask, the area of the polygon p200a will be defined as clear and surrounded by opaque areas. In addition, the layout manipulation program defines polygons p204, p206 and p208 that correspond to phase shift areas on the mask that together will create the two sub-wavelength gates 202a and 202b. The sizes of the polygons p204, p206, and p208 are minimized as compared with the size of the phase shifting regions 84, 86 and 88 created with conventional techniques as shown in FIGURE 2.

As indicated above, one embodiment of the present invention separates the polygons created into one of several data layers. Each polygon that corresponds to a conventional pattern on the mask is placed in one data layer as shown in FIGURE 6C. In addition, the polygons that define different phase shifting areas of a phase shifter are placed in different data layers. For example, polygons p204 and

p208 are placed in one data layer as shown in FIGURE 6D and the polygon p206 for the other phase shifting area is placed in another data layer as shown in FIGURE 6E.

Once the polygons associated with different phase shift areas are placed in separate data layers, the layout manipulation program makes a phase selection for the polygons in the data layers according to a desired design criteria. For example, if the design criteria specifies that the area of etched phase shift regions is to be minimized, the computer system sums the area of the polygons p204 and p208 within the data layer shown in FIGURE 6D and compares the total area with the summed area of the polygons contained in the data layer shown in FIGURE 6E. Depending upon which data layer has the polygons with the smallest summed area, those polygons can be selected to have a 180° etched phase shift. Once the computer system has made an initial phase shift selection for all the polygons in a data layer, a simulation can be performed on the circuit layout to ensure that the circuit will perform as desired.

As will be appreciated, depending upon the selection of the phase shift values for the various polygons that define the phase shifters, the appropriate trim masks can then be defined. For example, if the polygon p204 and p208 are selected to have 180° phase shifts, then subwavelength artifacts will be created in the areas 210 and 212 is shown by the dashed lines in FIGURE 6B. Therefore, a data layer that defines a trim mask as shown in FIGURE 6F can be created by the layout manipulation program. The trim mask is opaque except for the areas 220 and 222. Illumination of the wafer through the trim mask removes the undesired artifacts created at the boundaries of a 0° and 180° phase shift area. Alternatively, if the polygon p206 is selected to have a 180° phase shift, then artifacts will be created in the areas 214 and 216 shown by the dashed lines in FIGURE 6B. Therefore, a data layer that defines a trim mask as shown in FIGURE 6G is created. The trim mask is opaque except for areas 224 and 226.

As will be appreciated, trim masks are only required if 0° and 180° phase shifters are used. If alternate phase shifting schemes such as 90°/270° or 60°/120°phase shifters are used, then no trim masks need be created.

The present invention is not limited to optimizing phase shifters that lie side by side on the mask. As indicated above, phase shifting may be accomplished by using a attenuating phase shifting material on the mask to define circuit elements. Typically, these masks are made using a molybdenum silicide material, in which the thickness and optical properties are controlled to allow the transmission to be small, typically 6-9%, and phase shifted by 180°. In order to limit the total amount of light

that passes through the mask, portions of the attenuating material can be covered with an opaque chrome to form a tri-tone mask. FIGURE 7 illustrates a plan view of a portion of a mask wherein the mask contains a pattern of attenuating material, which is sometimes referred to as "leaky chrome". In addition some areas of the attenuating material may be covered with an opaque chrome 252. The present invention can optimize the placement of the opaque chrome over the leaky chrome by creating separate data layers for the polygons that define the leaky chrome areas and for the polygons that define the areas of opaque chrome. With the polygons for each area separated, the layout manipulation program can perform calculations to optimize the size of the opaque areas, while still getting the benefits of the phase shifting areas due to the light passing through the attenuating material. Once the polygons in each of the data layers have been optimized, the data layers are provided as input to the mask writer to create the different layers on the photolithographic mask.

While the preferred embodiment of the invention has been illustrated and described, it will be appreciated that various changes can be made therein without departing from the scope of the invention. For example, although use of the present invention is illustrated with respect to creating integrated circuits, it will be appreciated that the present invention can also be used to create micro electro-mechanical structures (MEMS), thin film disk drive heads or other structures created using photolithographic techniques. Similarly, data structures that define different areas of a phase shifter need not be grouped in different data layers. The data structures could be grouped in a common data layer and tagged with an identifier that allows the computer to identify it and perform an optimization calculation prior to assigning a phase shift value. Once the phase shift values are assigned, the different polygons for the phase shift areas having the same phase shift value are preferably written to a single data layer and provided to a mask processor such that the same process steps can be performed on each polygon in the data layer. It is therefore intended that the scope of the invention be determined from the following claims and equivalents thereto.